Raspberry Pi CM4

CM4 interfaces

File: cm4_io.kicad_sch

Pi CM4 – GPIO

File: cm4_gpio.kicad_sch

Pi CM4 – MPIO

File: cm4_mpio.kicad_sch

PTP_PPS

GNSS_PPS

UART3_TXD
UART3_RX
GNSS_RESET

REF_CLK_SEL

GPS

PTP_PPS
GNSS_PPS
GNSS_TX
GNSS_RX
GNSS_RESET
CLK_SEL

File: gps.kicad_sch

REF_CLK_P
REF_CLK_N

PLL_CLK_SEL
PLL1_SCL
PLL1_SDA
PLL2_SCL
PLL2_SDA
PLL_OE
PLL_LOCK
SFP_PRESENT
SFP_TX_DISABLE
SFP_LOS
SFP_TX_FAULT

PLL and SFP

CLK_SEL
PLL1_SCL
PLL1_SDA
PLL2_SCL
PLL2_SDA
PLL_OE
PLL_LOCK
SFP_SCL
SFP_SDA
SFP_PRESENT
SFP_TX_DISABLE
SFP_LOS_OD
SFP_TX_FAULT_OD

File: pll.kicad_sch

REF_CLK_P
REF_CLK_N

RF1
RF2
RF3
RF4
RF5
RF6
RF7
RF8

I2C Addresses:
SFP: 0x50
INA3221: 0x40
RC32504: 0x09

PWR_CRITICAL
PCIE_PWR_GOOD
3V3_SENSE_P
3V3_SENSE_N

Power Supplies

SCL
SDA
POWER_CRITICAL
PCIE_PGOOD
POWER_SENSE3_P
POWER_SENSE3_N

File: power.kicad_sch

UART0_RX
UART0_TX
RS485_RX/TX

RS485_RX
RS485_TX
RS485_R/W

STATUS_RED
STATUS_GREEN
COMMS_RED
COMMS_GREEN
ONEWIRE_ADDRESS

LD1
WP130WCP_2EGW

R1 1k0
R2 1k0
R3 1k0
R4 1k0

3V3
C1 10u 16V
C2 100n 25V
U1 Analog MAX3483ESA+
RS485_RX
RS485_R/W
RS485_TX
RS485_B
RS485_A
R5 120R

RS485_B
D10 3V3
12V
CN2A
Amphenol 86093488613755E1LF

RS485_A
D9 3V3
12V
CN2B
Amphenol 86093488613755E1LF

U2 DS2431P+
ONEWIRE_ADDRESS
D6 3V3
D22 3V3
12V
CN2C
Amphenol 86093488613755E1LF

CN1
Samtec GRF1-J-P-08-E-RA-TH1
D1 5V0
D2 5V0
D3 5V0
D4 5V0
D5 5V0
D7 5V0
D8 5V0
D11 5V0

LAYOUT1 2.7mm NPTH
LAYOUT2 2.7mm NPTH
LAYOUT3 2.7mm NPTH

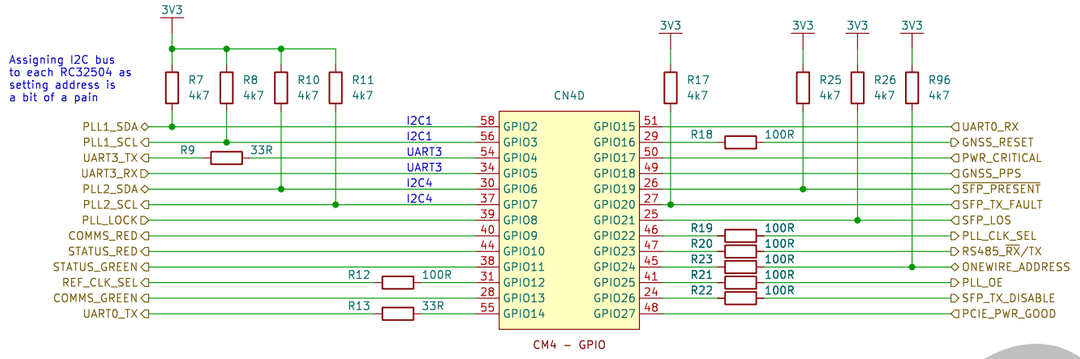
10mm Square Logo H1

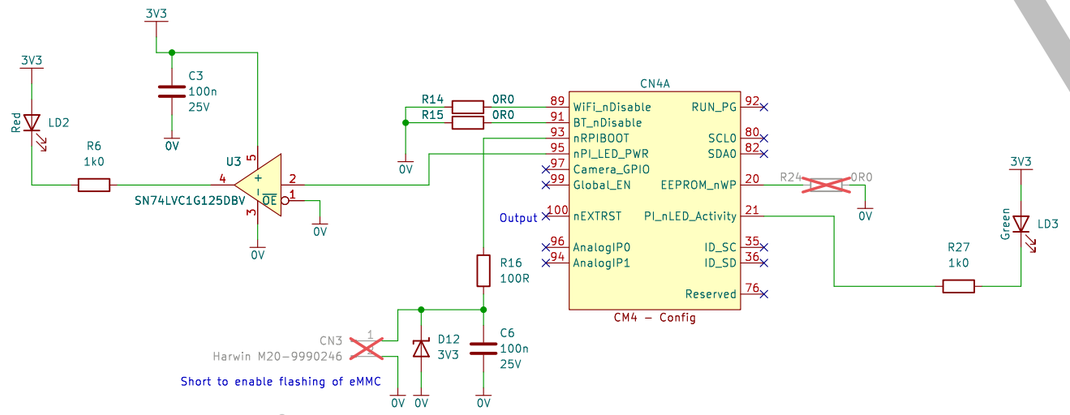
DRAFT

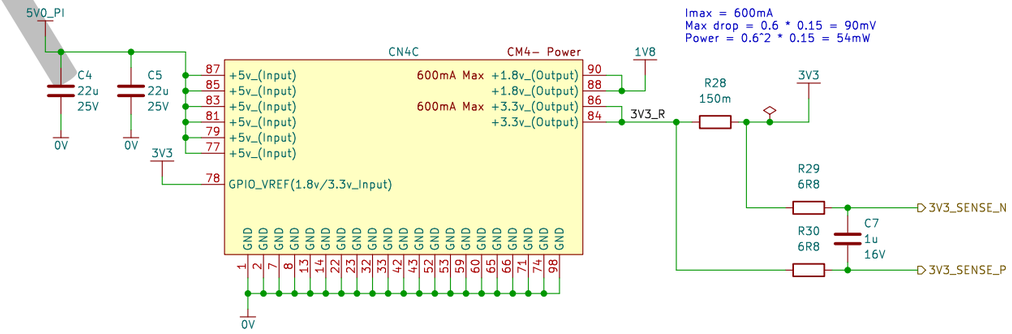
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File: Master Timing Card.kicad_sch

Title:

Size: A3	Date:	**Rev:**
KiCad E.D.A. 8.99.0-598-g7b935f7673		Id: 1/9

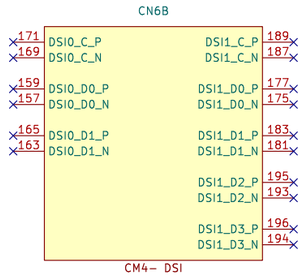


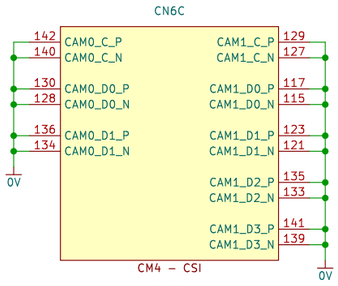


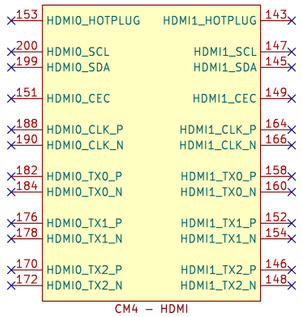


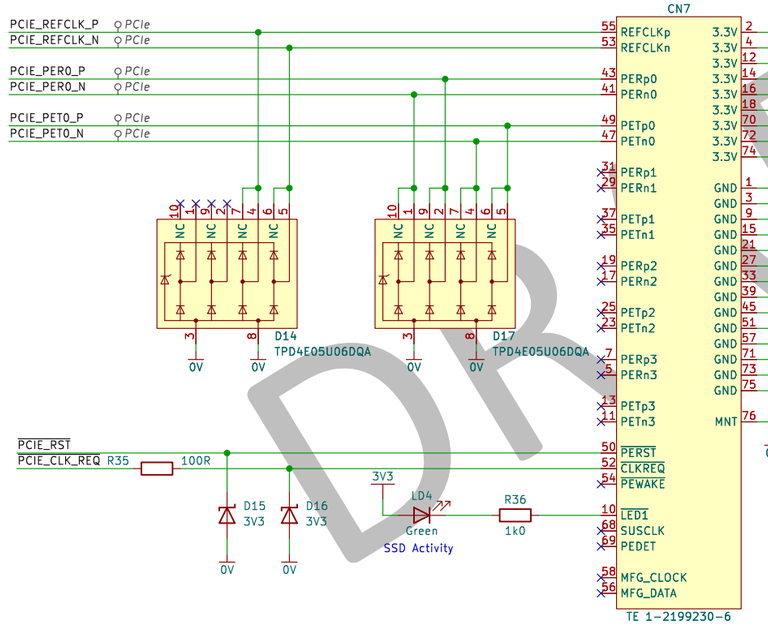
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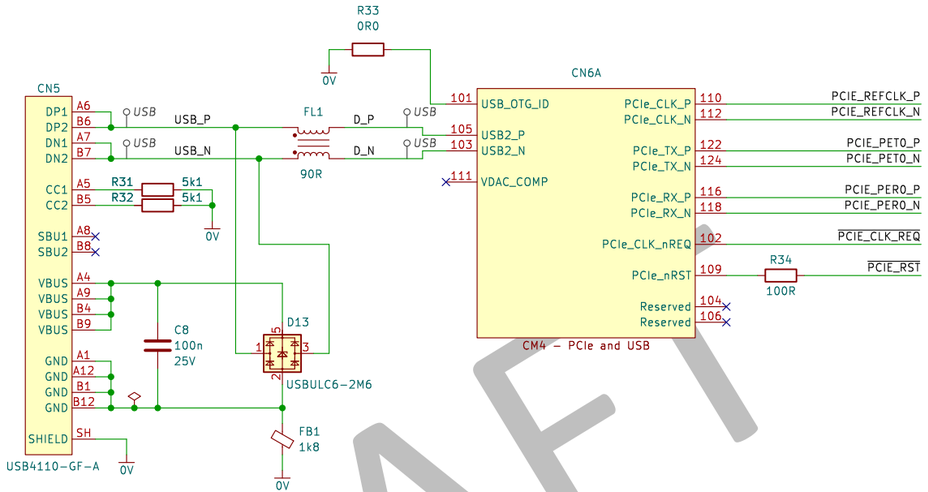
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File: cm4_gpio.kicad_sch		
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Size: A3	Date:	**Rev:**
KiCad E.D.A. 8.99.0-598-g7b935f7673		Id: 2/9

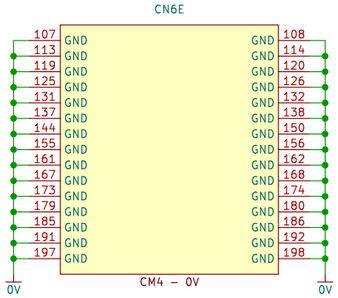












ZF1

Raspberry Pi
Compute Module 4

DRAFT

Sheet: /Pi CM4 – HPIO/	
File: cm4_hpio.kicad_sch	
Title:	
Size: A3	Date:
KiCad E.D.A. 8.99.0-598-g7b935f7673	Id: 3/9

H2
MS585-10C

SH1
MS585-10F

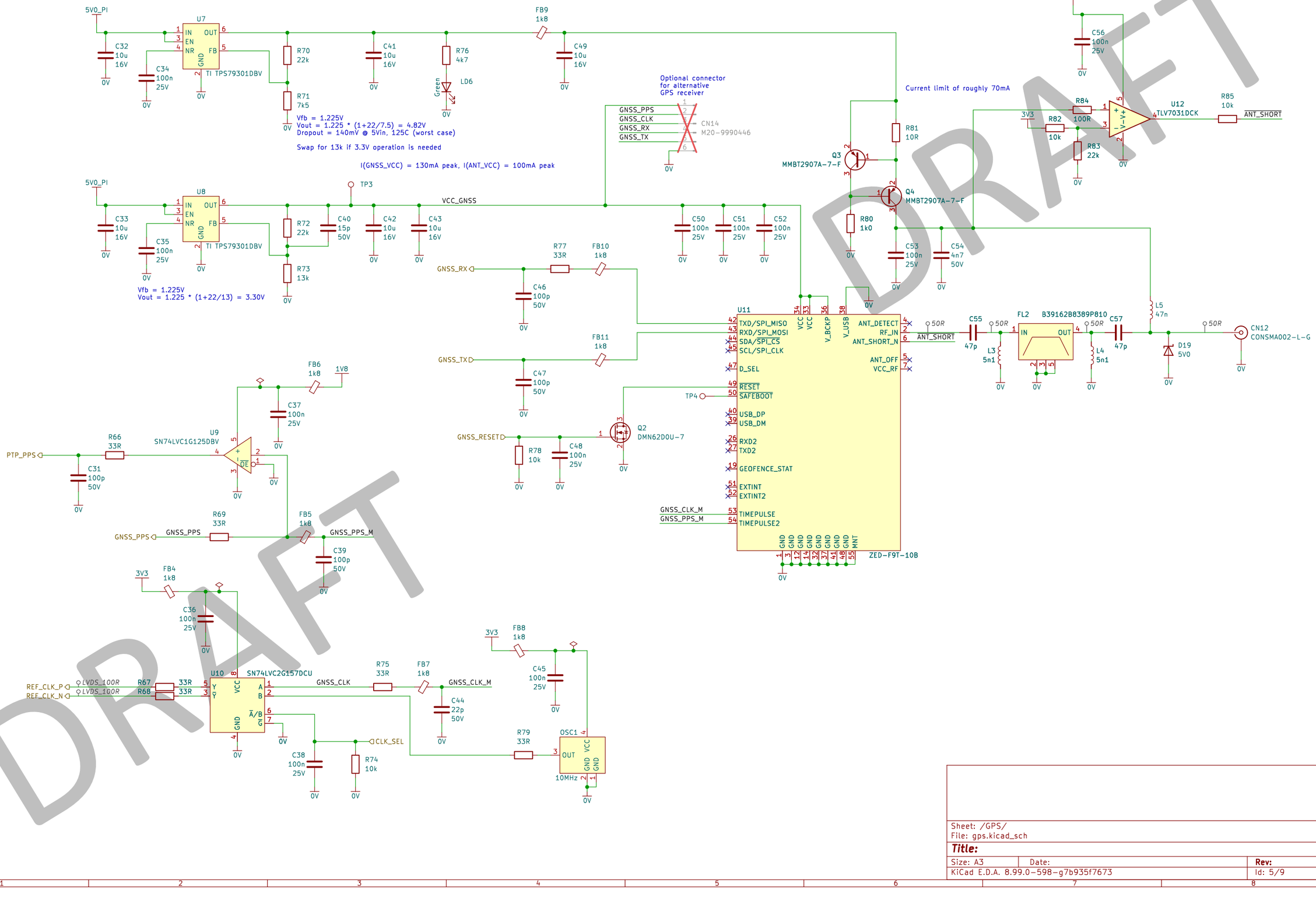
0V

Place resistors close to buffer IC

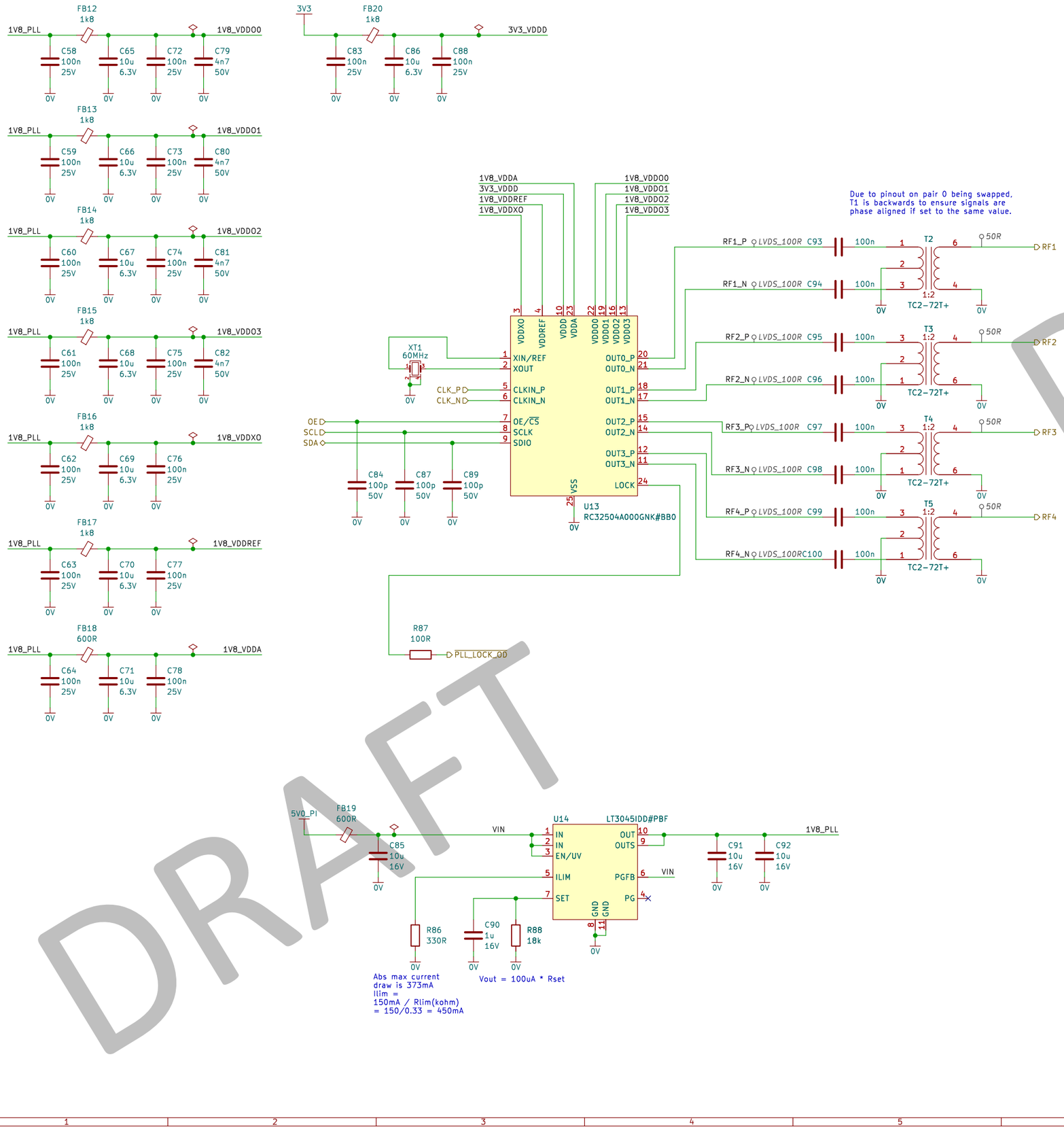
5V0_PI
FB2
600R
C11
10u
16V
C12
100n
25V
U4
IN
EN
NR
OUT
FB
GND
TI TPS79301DBV
TP1
VDD_MUX
R41
22k
C14
15p
50V
C15
10u
16V
C17
100n
25V
C18
100n
25V
R42
13k
Vfb = 1.225V
Vout = 1.225 * (1+22/13) = 3.30V
C13
100n
25V
R38
130R
R40
130R
R44
100R
U5
VDDIN
VDD
IN1_P
IN1_N
IN2_P
IN2_N
SEL
OE
PD
IREF
GND
CLKA_P
CLKA_N
CLKB_P
CLKB_N
CLKC_P
CLKC_N
CLKD_P
CLKD_N
SY75576LKY
SFP_REFCLK_P
SFP_REFCLK_N
REF_CLK_P
REF_CLK_N
CLK_SEL
Internal pullups
R37
82R
R39
82R
R43
10k
C16
100n
25V
R46
475R
R49
33R
R50
33R
R51
140R
R52
180R
R53
180R
R54
33R
R55
33R
R56
33R
R57
33R
R58
33R
R59
33R
LVDS_100R SFP_TX_P
LVDS_100R SFP_TX_N
HCSL_100R EXT_CLK_P
HCSL_100R EXT_CLK_N
HCSL_100R PLL1_CLK_P
HCSL_100R PLL1_CLK_N
HCSL_100R PLL2_CLK_P
HCSL_100R PLL2_CLK_N
3V3
FB3
600R
L1
1u0
L2
1u0
C23
10u
16V
C24
100n
25V
C27
100n
25V
C28
10u
16V
C30
100n
25V
CN11
VccR
VccT
TD+
TD−
RD−
RD+
Input
Output
SFP_TX_P
SFP_TX_N
SFP_REFCLK_P
SFP_REFCLK_N
R64
10R
R65
10R
REFCLK_R_P
REFCLK_R_N
SFP_TX_FAULT_OD
SFP_LOS_OD
TP2
SFP_SDA
SFP_SCL
SFP_PRESENT
I2C Address = 0x50
TX_FAULT
TX_DISABLE
RATE_SELECT
LOS
MOD_DEF2/SDA
MOD_DEF1/SCL
MOD_DEF0/GND
VeeR
VeeT
UE75-A20-6000T
SFP_TX_DISABLE
R60
10k
C22
100n
25V
Q1
DMN62D0U-7
C25
100p
100V
C26
100p
100V
C29
100p
100V
CN10
U77-A1114-30L1
Frequency Synthesiser 1
PLL1_CLK_P
PLL1_CLK_N
PLL1_SCL
PLL1_SDA
PLL_OE
CLK_P
CLK_N
SCL
SDA
OE
RF1
RF2
RF3
RF4
PLL_LOCK_OD
File: rc32504.kicad_sch
Frequency Synthesiser 2
PLL2_CLK_P
PLL2_CLK_N
PLL2_SCL
PLL2_SDA
R45
10k
R47
10k
C19
100n
25V
U6
SN74LVC1G02DCK
VCC
PLL_LOCK
R48
10k
LD5
Green
Should be 0.7V amplitude = 5mW
7.5dB attenuator to give just under 0dBm
EXT_CLK_P
EXT_CLK_N
C20
C21
100n
T1
1:2
TC2-72T+
50R
R61
20R
R62
51R
R63
20R
D18
5V0
CN9
731385033

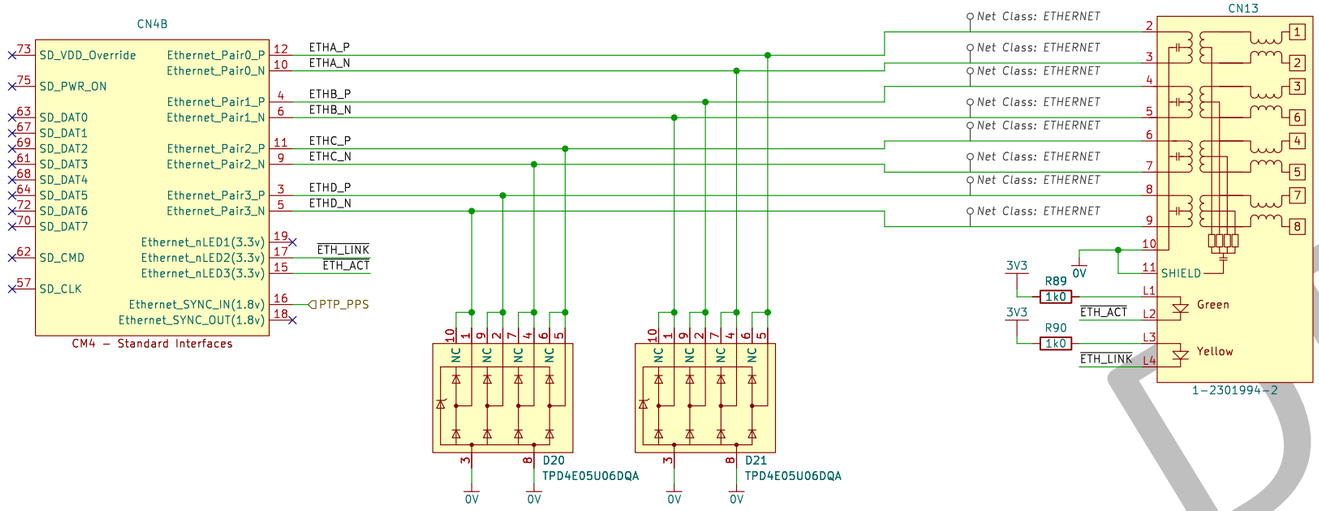
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File: pll.kicad_sch
Title:
Size: A3
Date:
Rev:
KiCad E.D.A. 8.99.0-598-g7b935f7673
Id: 4/9



Sheet: /GPS/	
File: gps.kicad_sch	
Title:	
Size: A3	Date:
KiCad E.D.A. 8.99.0-598-g7b935f7673	**Rev:** Id: 5/9

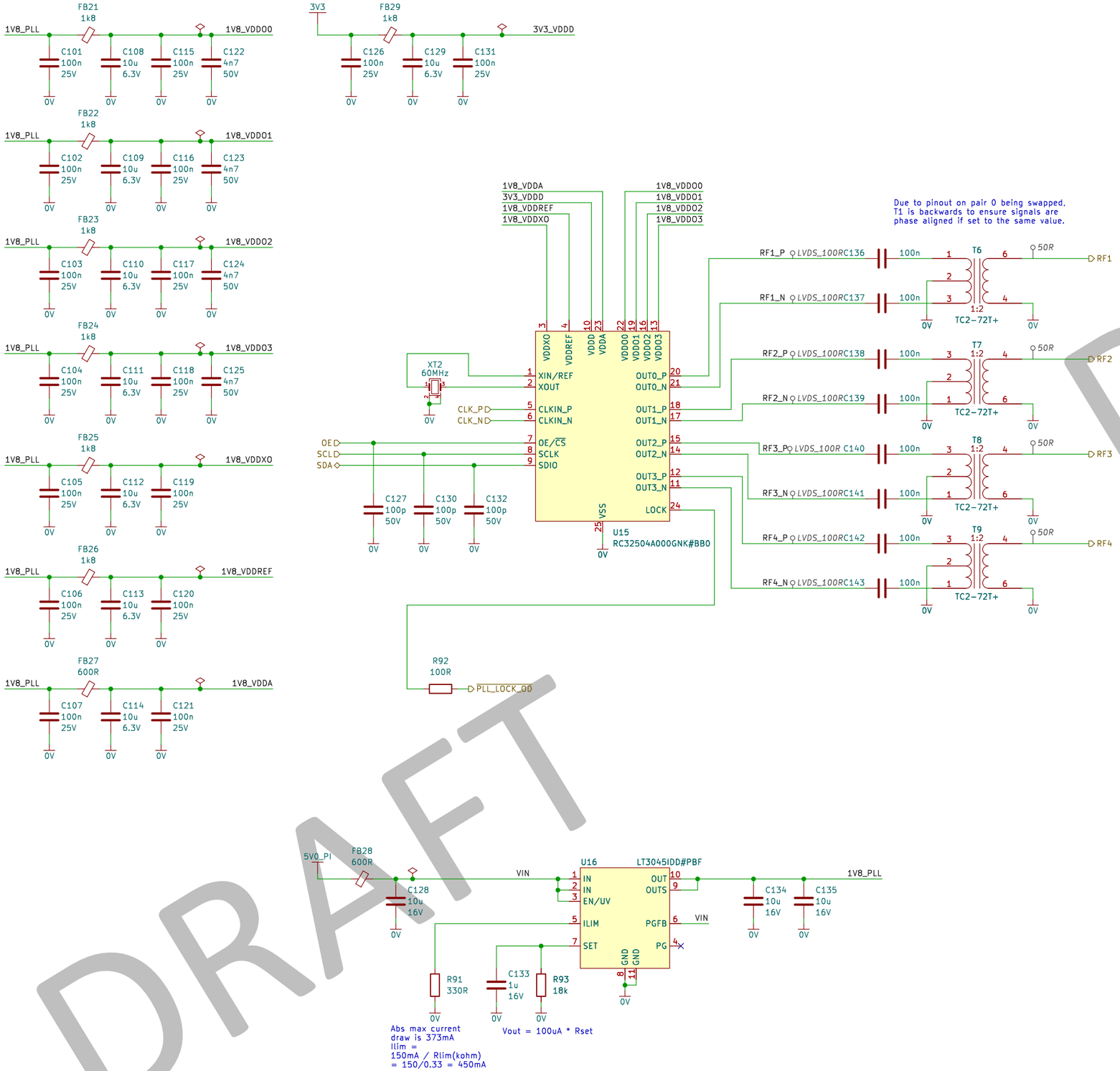

FB12
1k8
1V8_PLL
1V8_VDDO0
C58
100n
25V
C65
10u
6.3V
C72
100n
25V
C79
4n7
50V
0V
FB13
1k8
1V8_PLL
1V8_VDDO1
C59
100n
25V
C66
10u
6.3V
C73
100n
25V
C80
4n7
50V
FB14
1k8
1V8_PLL
1V8_VDDO2
C60
100n
25V
C67
10u
6.3V
C74
100n
25V
C81
4n7
50V
FB15
1k8
1V8_PLL
1V8_VDDO3
C61
100n
25V
C68
10u
6.3V
C75
100n
25V
C82
4n7
50V
FB16
1k8
1V8_PLL
1V8_VDDXO
C62
100n
25V
C69
10u
6.3V
C76
100n
25V
FB17
1k8
1V8_PLL
1V8_VDDREF
C63
100n
25V
C70
10u
6.3V
C77
100n
25V
FB18
600R
1V8_PLL
1V8_VDDA
C64
100n
25V
C71
10u
6.3V
C78
100n
25V
3V3
FB20
1k8
3V3_VDDD
C83
100n
25V
C86
10u
6.3V
C88
100n
25V
1V8_VDDA
3V3_VDDD
1V8_VDDREF
1V8_VDDXO
1V8_VDDO0
1V8_VDDO1
1V8_VDDO2
1V8_VDDO3
VDDXO
VDDREF
VDDD
VDDA
VDDO0
VDDO1
VDDO2
VDDO3
XT1
60MHz
XIN/REF
XOUT
CLK_P
CLK_N
CLKIN_P
CLKIN_N
OE
SCL
SDA
OE/CS
SCLK
SDIO
OUT0_P
OUT0_N
OUT1_P
OUT1_N
OUT2_P
OUT2_N
OUT3_P
OUT3_N
LOCK
VSS
C84
100p
50V
C87
100p
50V
C89
100p
50V
U13
RC32504A000GNK#BB0
Due to pinout on pair 0 being swapped,
T1 is backwards to ensure signals are
phase aligned if set to the same value.
RF1_P
RF1_N
RF2_P
RF2_N
RF3_P
RF3_N
RF4_P
RF4_N
LVDS_100R
C93
C94
C95
C96
C97
C98
C99
C100
100n
T2
T3
T4
T5
1:2
TC2-72T+
50R
RF1
RF2
RF3
RF4
R87
100R
PLL_LOCK_OD
5V0_Pi
FB19
600R
VIN
U14
LT3045IDD#PBF
IN
EN/UV
ILIM
SET
OUT
OUTS
PGFB
PG
GND
C85
10u
16V
C91
10u
16V
C92
10u
16V
R86
330R
C90
1u
16V
R88
18k
Abs max current
draw is 373mA
Ilim =
150mA / Rlim(kohm)
= 150/0.33 = 450mA
Vout = 100uA * Rset
DRAFT
Sheet: /PLL and SFP/Frequency Synthesiser 1/
File: rc32504.kicad_sch
Title:
Size: A3
Date:
Rev:
KiCad E.D.A. 8.99.0-598-g7b935f7673
Id: 6/9

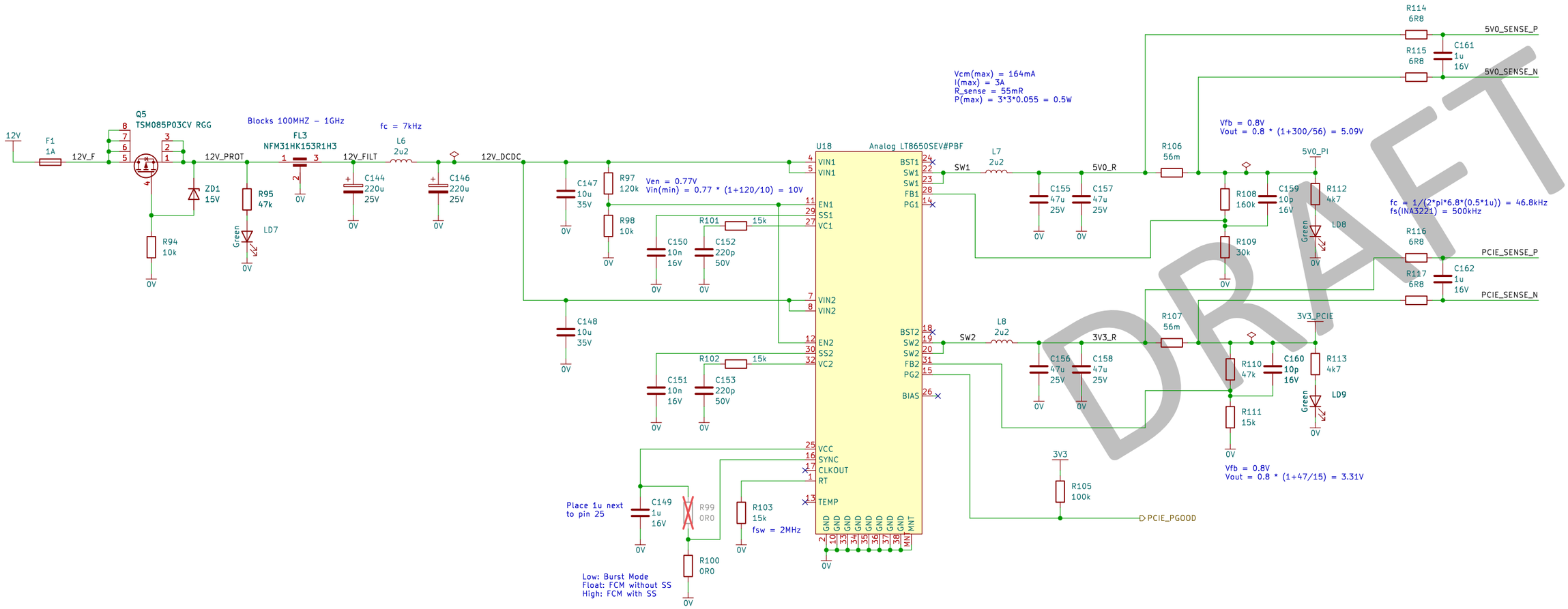


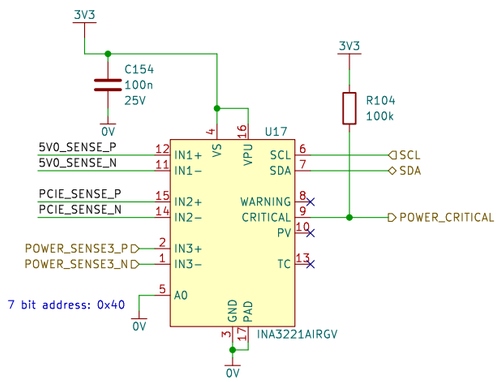
DRAFT

DRAFT

Sheet: /CM4 Interfaces/		
File: cm4_io.kicad_sch		
Title:		
Size: A3	Date:	**Rev:**
KiCad E.D.A. 8.99.0-598-g7b935f7673		Id: 7/9


FB21
1k8
1V8_PLL
1V8_VDDO0
C101
100n
25V
C108
10u
6.3V
C115
100n
25V
C122
4n7
50V
0V
FB22
1k8
1V8_PLL
1V8_VDDO1
C102
100n
25V
C109
10u
6.3V
C116
100n
25V
C123
4n7
50V
0V
FB23
1k8
1V8_PLL
1V8_VDDO2
C103
100n
25V
C110
10u
6.3V
C117
100n
25V
C124
4n7
50V
0V
FB24
1k8
1V8_PLL
1V8_VDDO3
C104
100n
25V
C111
10u
6.3V
C118
100n
25V
C125
4n7
50V
0V
FB25
1k8
1V8_PLL
1V8_VDDXO
C105
100n
25V
C112
10u
6.3V
C119
100n
25V
0V
FB26
1k8
1V8_PLL
1V8_VDDREF
C106
100n
25V
C113
10u
6.3V
C120
100n
25V
0V
FB27
600R
1V8_PLL
1V8_VDDA
C107
100n
25V
C114
10u
6.3V
C121
100n
25V
0V
3V3
FB29
1k8
3V3_VDDD
C126
100n
25V
C129
10u
6.3V
C131
100n
25V
0V
1V8_VDDA
3V3_VDDD
1V8_VDDREF
1V8_VDDXO
1V8_VDDO0
1V8_VDDO1
1V8_VDDO2
1V8_VDDO3
VDDXO
VDDREF
VDDD
VDDA
VDDO0
VDDO1
VDDO2
VDDO3
XT2
60MHz
XIN/REF
XOUT
CLK_P
CLK_N
CLKIN_P
CLKIN_N
OE
SCL
SDA
OE/CS
SCLK
SDIO
OUT0_P
OUT0_N
OUT1_P
OUT1_N
OUT2_P
OUT2_N
OUT3_P
OUT3_N
LOCK
VSS
C127
100p
50V
C130
100p
50V
C132
100p
50V
U15
RC32504A000GNK#BB0
R92
100R
PLL_LOCK_OD
Due to pinout on pair 0 being swapped,
T1 is backwards to ensure signals are
phase aligned if set to the same value.
RF1_P
RF1_N
RF2_P
RF2_N
RF3_P
RF3_N
RF4_P
RF4_N
LVDS_100RC136
LVDS_100RC137
LVDS_100RC138
LVDS_100RC139
LVDS_100R C140
LVDS_100RC141
LVDS_100RC142
LVDS_100RC143
100n
T6
T7
T8
T9
1:2
TC2-72T+
50R
RF1
RF2
RF3
RF4
5V0_Pi
FB28
600R
VIN
U16
LT3045IDD#PBF
IN
IN
EN/UV
ILIM
SET
OUT
OUTS
PGFB
PG
GND
GND
C128
10u
16V
C133
1u
16V
C134
10u
16V
C135
10u
16V
R91
330R
R93
18k
1V8_PLL
Abs max current
draw is 373mA
Ilim =
150mA / Rlim(kohm)
= 150/0.33 = 450mA
Vout = 100uA * Rset
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Id: 8/9





DRAFT

Sheet: /Power Supplies/ File: power.kicad_sch		
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Size: A3	Date:	**Rev:**
KiCad E.D.A. 8.99.0-598-g7b935f7673		Id: 9/9